

800.0039

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Pechanek et al.

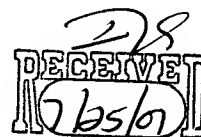
Serial No.: 09/422,015

Filed: October 21, 1999

For: METHODS AND APPARATUS FOR
ABBREVIATED INSTRUCTION AND
CONFIGURABLE PROCESSOR
ARCHITECTURES^S *SETS ADAPTABLE TO*

Group: 2183

Examiner: K. Kim



OFFICIAL

Chapel Hill, North Carolina
April 23, 2001Assistant Commissioner For Patents
Washington, DC 20231Amendment

Please amend the above identified application as follows:

In the SpecificationPlease replace the paragraph beginning at page 2, line 4, with the following rewritten
paragraph:

In order to meet these opposing requirements, it is necessary to develop a processor architecture and apparatus that can be configured in more optimal ways to meet the requirements of the intended task. One prior art approach for configurable processor designs uses field programmable gate array (FPGA) technology to allow software-based processor optimizations of specific functions. A critical problem with this FPGA approach is that standard designs for high